Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte BRIAN K. KONIGSBURG, GEORGE M. LATTIMORE
and JOHN S. MUHICH

_____

Appeal No. 1999-2747
Application 08/757,979

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ON BRIEF

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Before BARRETT, FLEMING and LEVY, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-5, 9-14 and 18-21. The rejection of claim 19 was later withdrawn.[1] Claims 6-8 and 15-17 have been canceled.

Appellants' invention relates to a method and apparatus

[1]Examiner's Answer, page 2.

for controlling the operation of a storage array after a failure in the storage array (specification, page 4, lines 2-6). Cache memory array (specification, page 6, lines 30-31; figure 2, numeral 20) includes a tag array (figure 2, numeral 30) and a data array (figure 2, numeral 50). An address (figure 2, numeral 22), including a tag portion (figure 2, numeral 24) and an index portion (figure 2, numeral 26), is presented to the cache array for selection of a cache line for storage or retrieval of data in the data array (specification, page 6, line 31, through page 7, line 5).

The tag bit outputs from the address are connected to respective inputs of a comparator (figure 2, numeral 28) wherein address information from the tag array is compared with the tag portion of the address (specification, page 7, lines 5-8). Each line in the tag array includes set fields (figure 2, numeral 34) which include a tag portion (figure 2, numeral 36), a MESI field (figure 2, numeral 38) and a least recently used field (figure 2, numeral 40) (specification, page 7, lines 12-15). The tag field for the selected line is output to the comparator for comparison with the tag portion of the input address to determine if there is a match between

a desired line, as indicated by the address, in the contents of the array, as indicated by the tag fields in the tag array (specification, page 7, lines 15-20).

The MESI field Invalid flag is used to inhibit access to a cache set for which one or more failures have been determined (specification, page 7, lines 22-27). The data for the selected line from the data array is output to multiplexer (figure 2, numeral 52) where a selected set data is gated as cache data out on a line (figure 2, numeral 54) under control of encoder (figure 2, numeral 44) which encodes the output of the comparator (specification, page 8, lines 10-14). If the invalid flag in the MESI field is on, a corresponding set of data in the data array is inhibited and will not pass through the multiplexer to the cache data output line (specification, page 8, lines 16-19).

Independent claim 20 is reproduced as follows:

20. A method for controlling operation of a storage array after a failure comprising the steps of:

identifying a failing element in the storage array;

setting a flag to inhibit access to a portion of the array accessed by the failing element; and

storing to and retrieving data from remaining portions of the array, wherein the step of setting a flag comprises setting a set invalid bit in a flag field of a line in the storage array.

The references relied on by the Examiner are as follows:

Lefsky et al. (Lefsky)	5,019,971	May 28, 1991
McClure	5,708,789	Jan. 13, 1998 (filed Sep. 20, 1996)

Handy, The Cache Memory Book, ISBN 0-12-322985, (Academic Press, Inc. 1993). pages 158-161

Claims 1-5, 9-14, 18 and 20-21 stand rejected under 35 U.S.C. § 103 as being unpatentable over Lefsky when taken with McClure and Handy.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Brief,[2] Reply Brief,[3] and Answer[4] for the respective details thereof.

OPINION

After a careful review of the evidence before us, we agree with the Examiner that claims 1, 4, 5, 10, 13, 14 and 20-21 are unpatentable under 35 U.S.C. § 103 over Lefsky,

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[2]The Brief was received February 1, 1999.

[3]The Reply Brief was received May 27, 1999.

[4]The Answer was mailed March 25, 1999.

McClure and Handy.

At the outset, we note that Appellants have indicated on page 3, section VI, of the brief that claims 1, 4, 5, 9, 10, 13, 14, 18, 20 and 21 form a single group, and does not include a statement that the claims of this group do not rise and fall together. We further note that Appellants have argued all the claims in this group together and have not explained why the claims of this group are believed to be separately patentable. 37 CFR § 1.192 (c)(7)(July 1, 1998) ***as amended at*** 62 Fed. Reg. 53196 (October 10, 1997), which was controlling at the time of Appellants filing the brief, states:

> For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.

Appellants have not provided a statement that the claims

stand or fall together in regard to the above groups. We will, thereby, consider this group of Appellants' claims as standing or falling together, and we will treat claim 20 as a representative claim of that group.

Appellants argue[5] generally that the limitations of these claims are not suggested by the prior art. Specifically, Appellants point to claims 1, 10 and 19 which recite that after a failing element has been identified in a storage array, an Invalid bit in the MESI field of a cache line in the storage array will be set to inhibit access to the portion of the array accessed by the failing element. Appellants then note that the Examiner has admitted that Lefsky does not teach the operation of a cache supporting the MESI protocol or the use of an Invalid bit to set a flag to inhibit access to a portion of the storage array accessed by the failing element.

Turning to McClure, Appellants assert that this reference fails to disclose the setting of a flag to inhibit access to a portion of the storage array accessed by the failing element, wherein the setting of the flag comprises the setting of an

[5]Brief, page 4.

Invalid bit in the MESI field of a cache line in the storage array.

Appellants then argue[6] that the Examiner's citation of Handy to teach that the MESI cache protocol is a common protocol and its use would have been obvious to one of ordinary skill in this art, is merely an unsupported opinion of the Examiner and is without objective support. Appellants assert that the present invention utilizes the MESI protocol in a unique manner heretofore not known.

In his Answer,[7] the Examiner finds that Lefsky discloses a high availability set associative cache whereby defective portions of the cache are identified at a granularity of the cell level during cache operation, and a flag in the form of a force bit is set to indicate the defective cell(s). The cells which are flagged defective are mapped out and allow the remainder of the cache to function despite the presence of defective cell(s).

Turning to McClure, the Examiner posits that this

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[6]Brief, pages 5-7.

[7]Answer, pages 5 and 8.

reference teaches that defective cache locations may be mapped out using validity bits, because forcing a validity bit to indicate that the defective location does not contain valid data would force a main memory access instead of a cache access, thereby effectively bypassing the cache only for those locations which contain defective or invalid data.

Handy is cited by the Examiner to teach that the MESI cache protocol is a common protocol. The Examiner then asserts that an artisan at the time the invention was made would have realized that the Invalid bit of a cache using the MESI protocol is the same Invalid bit used in non-MESI protocol caches to indicate whether a particular cache location is valid.

As pointed out by our reviewing court, we must first determine the scope of the claim. "[T]he name of the game is the claim." ***In re Hiniker Co.***, 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

We therefore consider claim 20 to determine its scope. The preamble of this claim reads: "A method for controlling operation of a storage array after a failure comprising the

steps of." This limitation is met by the Lefsky disclosure[8] of a cache memory wherein status bits for mapping out defective cache cells and for controlling cache memory data replacement are stored.

The first subparagraph of this claim reads: "identifying a failing element in the storage array." Lefsky, discloses[9] that if a cache cell experiences a failure, the failure is detected by the read circuitry and a force bit is set to indicate a defective cache cell. Thus, this section of the claim is disclosed by Lefsky.

The third subparagraph of this claim reads: "setting a flag to inhibit access to a portion of the array accessed by the failing element." Lefsky discloses[10] that when cache cell failure is detected, a force bit is set to indicate a defective cache cell and thereafter no data is stored in that cache cell and its inputs are ignored. The force bit is the herein claimed flag which inhibits access to a portion of the

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[8]Column 1, lines 7-13.

[9]Column 5, lines 13-16.

[10]Column 5, lines 13-18.

array.

The final subparagraph of this claim reads: "storing to and retrieving data from remaining portions of the array, wherein the step of setting a flag comprises setting a set invalid bit in a flag field of a line in the storage array." Lefsky discloses[11] that his system maps out defective cache cells so that operation of the rest of the cache system can continue, and[12] that the output enable means suppresses a cache cell output when the force bit is set so that as long as one cache cell in each set of the cache memory remains operational, the system can continue operation. Furthermore, the force bit is clearly the set invalid bit in a flag field of a line in the storage array of Lefsky.

Therefore, upon considering Lefsky as a whole, we find that Lefsky discloses all of the limitations of claim 20. As we have found above that Lefsky, discloses all the limitations of claim 20, this claim is obvious over Lefsky. "[A] disclosure that anticipates under Section 102 also renders the

[11]Column 12, lines 65-67.

[12]Column 3, lines 9-24.

claim invalid under Section 103, for 'anticipation is the epitome of obviousness.'" ***Connell v. Sears, Roebuck & Co.***, 722 F.2d 1542, 1548, 220 USPQ 193, 198 (Fed. Cir. 1983) (**citing *In re Fracalossi***, 681 F.2d 792, 215 USPQ 569 (CCPA 1982)). We note that Appellants have not argued that Lefsky has failed to meet any of the aforesaid limitations of claim 20. We are not required to raise and/or consider such issues. As stated by our reviewing court in ***In re Baxter Travenol Labs.***, 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991), "[i]t is not the function of this court to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art." 37 CFR § 1.192(a) as amended at 62 FR 53196 Oct. 10, 1997, which was controlling at the time of Appellants' filing the brief, states as follows:

> The brief . . . must set forth the authorities and arguments on which the appellant will rely to maintain the appeal. Any arguments or authorities not included in the brief may be refused consideration by the Board of Patent Appeals and Interferences, unless good cause is shown.

Thus, 37 CFR § 1.192 provides that just as the court is not under any burden to raise and/or consider such issues this

board is not under any greater burden.

As Appellants have indicated on page 3, section VI, of the brief that claims 1, 4, 5, 9, 10, 13, 14, 18, 20 and 21 form a single group, and do not include a statement that the claims of this group do not rise and fall together, the decision of the Examiner rejecting claims 1, 4, 5, 9, 10, 13, 14, 18, 20 and 21 under 35 U.S.C. § 103 is affirmed.

As regards claims 2-3 and 11-12, these claims recite that the failing element recited in their parent claims is a memory bit line or a memory word line. The Examiner admits[13] that both bit lines and word lines are at a granularity level larger than the cell which is used in Lefsky, and points to McClure where memory access typically occurs at a granularity level larger than that of a single cell. The Examiner then posits that it would take less circuitry to flag faulty memory at either the word line or bit line levels than it would do so at the cell level. The Examiner then asserts that it would have been obvious to have chosen an error detection and bypassing mechanism which operates at the claimed granularity

[13]Examiner's Answer, page 6.

levels because it would make the system more economical by reducing the amount of circuitry required to bypass faults at the cost of bypassing a greater amount of the cache since this would not result in any performance degradation if the data is accessed in amounts no more than the claimed granularity levels.

As an additional basis for this assertion, the Examiner states:[14] "In the highly competitive world of computer systems . . . artisans constantly strive to reduce cost while maximizing functionality. Making a particular memory design more economical, especially if it can be done without performance degradation, is an important consideration in an industry where prices are constantly falling."

Appellants argue[15] that just because a solution is more economical does not mean the solution is therefore obvious, and state that the Examiner's assertions amount to an unsupported opinion by not having objective support to back the "economical" assertion.

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[14]Examiner's Answer, page 12.

[15]Brief, page 10; Reply Brief, page 2.

As regards claims 2, 3, 11 and 12, we find that the Examiner has failed to set forth a ***prima facie*** case. As we stated above, it is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be

established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg., Inc. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***citing W. L. Gore & Assocs.***, 721 F.2d 1551, 1553, 220 USPQ 311, 312-13. In addition, our reviewing court requires the Patent and Trademark Office to make specific findings on a suggestion to combine prior art references. ***In re Dembiczak,*** 175 F.3d 994, 1000-01, 50 USPQ2d 1614, 1617-19 (Fed. Cir. 1999).

Therefore, mere economical benefit in a competitive industry is inadequate to support the rejection of claims 2, 3, 11 and 12 under 35 U.S.C. § 103.

Accordingly, the decision of the Examiner rejecting claims 1, 4, 5, 9, 10, 13, 14 and 20-21 under 35 U.S.C. § 103 as being unpatentable over Lefsky when taken with McClure and Handy is

affirmed, and the decision of the Examiner rejecting claims 2, 3, 11 and 12 under 35 U.S.C. § 103 as being unpatentable over

Lefsky when taken with McClure and Handy is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED IN PART

LEE E. BARRETT Administrative Patent Judge	)
MICHAEL R. FLEMING Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
STUART S. LEVY Administrative Patent Judge	)

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